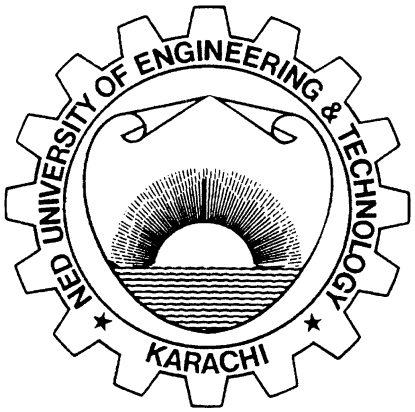
Practical Workbook
CS-431
Digital System Design



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Department of Computer & Information Systems Engineering
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INTRODUCTION

This workbook has been compiled to assist the conduct of practical classes for CS-431 Digital System Design. The practical workbook for "Digital System Design" introduces the basic as well as advanced concepts of digital system design using a Hardware Description Language (HDL). Verilog has been selected for this purpose because it has a C like syntax and so it is widely used in microchip industry for design and simulation of digital systems. A brief introduction of Verilog HDL is provided in the appendix A. Each lab session begins with a brief theory of the topic.

The Course Profile of CS-431 Digital System Design lays down the following Course Learning Outcome:

CLO-3: **"Practice** interfacing of FPGA boards and sensors for digital system design (P3, PLO-5)"

All lab sessions of this workbook have been designed to assist the achievement of the above CLO. Rubric sheets to evaluate student performance in psychomotor domains have been provided at the end of the workbook.

Lab session 1 is designed to explore Xilinx Vivado Development Environment for configuring FPGAs using Verilog HDL. Next three lab sessions are centered on synthesizing and simulating combinational circuits using gate level and dataflow modeling techniques. Lab 5 focuses on behavioral modeling and the next lab is designed to provide a practical knowledge to the students about implementing finite state machines (FSMs) and sequential circuits which play a very important role in the design of digital circuits. Lab session 7 covers the topic of PIPO-SISO shift register implementation. In Lab session 8, Read Write Memory (RWM) module is going to be designed and simulated. Lab session 9 allows students to learn about configuring built in IP Cores to use Block RAM (BRAM) of Xilinx FPGA.

Lab sessions 10 through 13 are performed on FPGA board to cover psychomotor domain at "Guided Response" level. These labs are implemented on Digilent Nexys A7, which is a ready to use digital circuit development board based on the latest Artix-7 FPGA from Xilinx. Lab 10 demonstrates how to assign the available on board IOs i.e., switches and LEDs, as input and output to the adder circuit. Lab 11 is related to driving tri-color LEDs control for illuminating them in red, green or blue color combinations. In Lab 12, students will interface 7 segment displays on Nexys A7. Lab 13 assigns the task of reading on-board temperature sensor data, interfaced using I^2C serial communication protocol, and displaying the result on time multiplexed on-board seven-segment displays. Lab 14 is a complex engineering activity based on implementing a digital system on an FPGA.

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