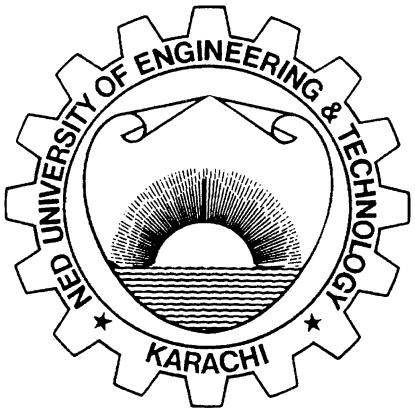
Practical Workbook
CS-319
VLSI Design



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Dept. of Computer & Information Systems Engineering
NED University of Engineering & Technology

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INTRODUCTION

This workbook has been compiled to assist the conduct of practical classes for CS-319 VLSI Design. The Practical Workbook for "VLSI Design" introduces the basic as well as advanced concepts of VLSI Design using a Hardware Description Language (HDL). Verilog has been selected for this purpose because it is widely used in microchip industry for design and simulation of digital systems. The brief introduction of Verilog HDL and Simulation tools is provided in the Appendix. Each lab session begins with a brief theory of the topic.

The Course Profile of CS-319 VLSI Design lays down the following Course Learning Outcome:

"CLO-1: **Explore** concepts and techniques used in VLSI circuit design and integrated circuit fabrication (C3, PLO-2)

CLO-3: **Practice** use of modern tools and techniques for memory and processor design using a hardware description language (Lab work) (P3, PLO-5)"

All lab sessions of this workbook have been designed to assist the achievement of the above CLOs. Rubric sheets to evaluate student performance both in cognitive as well as psychomotor domains have been provided at the end of the workbook.

Lab session 1 is to explore Xilinx ISE Development Environment for configuring FPGAs using Verilog HDL. Next two lab sessions are centered on synthesizing and simulating combinational circuits using gate level and dataflow modeling techniques. In Lab session 4, students are going to construct and simulate a three-way light control switch. Lab 5 focuses on behavioral modeling and the next two labs are designed to provide a practical knowledge to the students about implementing Finite State machines and sequential circuits which play a very important role in VLSI design of digital circuits. Lab session 8 covers the topic of PIPO-SISO shift register implementation. In Lab session 9, Read Write Memory Module (RAM) is going to be constructed and simulated. Lab session 10 allows students to learn about configuring built in IP Cores to use Block RAM (BRAM) of Xilinx FPGA.

Last four labs are performed on hardware to cover psychomotor domain at "Guided Response" level. These labs are implemented on Digilent Nexys4, which is a ready to use digital circuit development board based on the latest Artix-7 FPGA from Xilinx. In Lab 11, students will interface 7 segment display on Nexys4. Lab 12 is about driving tri-color LEDs control for illuminating them in red, green or blue colors. Lab 13 assigns available on board IOs i.e. switches and LEDs, as input and output to the adder circuit. Lab 14 is to interface temperature sensors. It reads analog values obtained by the temperature sensor IC and to generate its correspondence value in digital form.

This workbook is designed to assist both instructor and student, practically realizing theoretical concepts of the course, and providing in-depth understanding.

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