Practical Workbook
CS-221
Computer Organization & Design

Name : _____

Year : _____

Batch : _____

Roll No : _____

Department: _____

Department of Computer & Information Systems Engineering
NED University of Engineering & Technology

Practical Workbook
CS-221
Computer Organization & Design

Prepared by:
Ms. Anita Ali, Ms. Ramish Fatima, Ms. Mehwish Raza

Revised in:

February 2021

Revision 2

Department of Computer & Information Systems Engineering
NED University of Engineering & Technology

INTRODUCTION

This workbook has been compiled to assist the conduct of labs for CS-221 Computer Organization and Design. Practical work relevant to this course aims at providing students a chance to interact with various simulation tools to practice and learn various aspects of Instruction Set Architectures and Computer Organization. This workbook assists instructor and student in practical realization of theoretical concepts of the course, and provides in-depth understanding and elaborate system programming experience. The labs are intended to be thought provoking so that students can think out-of-the- box and have their own way of solving a problem rather than following the traditional footsteps. This is what makes the most exciting area of Computer Organization and Design!

The Course Profile of CS-221 Computer Organization and Design lays down the following Course Learning Outcome:

"Demonstrate the use of simulation tools for various Instruction Set Architectures (C3, PLO-5)"

All labs of this workbook have been designed to assist the achievement of the above CLO. A rubric to evaluate student performance has been provided at the end of the workbook.

In the first seven labs, QtSPIM is used to give students firm grasp of assembly language of MIPS processor, an essential component of many embedded systems. MIPS is an example of RISC (Reduced Instruction Set Computer) design wherein every feature of ISA (e.g. number of instructions in the instruction set, instruction formats, addressing modes) is reduced leading to a simple processor.

In next five labs, LogiSim has been introduced, which is a simulation tool for designing and simulating digital logic circuits. It is used to construct and simulate entire CPUs for educational purposes. Using LogiSim students can simulate datapath of MIPS processor (or its subset) and manipulate the design for them, thus getting a profound insight of processor design according to its Instruction Set Architecture. The last lab incorporates a cache simulator – Cache 351, to help students better understand cache mapping techniques and write policies.

CONTENT